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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,874	12/29/2000	Lily P. Looi	2207/9869	1458

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,874	LOOI ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12/29/00 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6,7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

Claims 13 and 22 are objected to because of the following informalities: there is no period at the end of the sentence. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 recites the limitation "the second scalability port switch" in the first and continuing on to the second line of the claims. There is insufficient antecedent basis for this limitation in the claim.

Claims 13 and 22 recites the limitation "the scalability port switch" in the last line of the claims. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Tavallaei et al.(US Patent 5,987,538), hereinafter referred to as Tavallaei.

Regarding claim 1, Tavallaei discloses an interrupt delivery system that has a first pair of scaleable node controllers(Figure 2, Component 14), wherein each node

controller supports at least 1 microprocessor(Figure 2, Components 12). Tavallaei further discloses a switch(Figure 2, Component 26) that receives an interrupt, determines an address of the node controller and sends the interrupt to that node controller. Tavallaei shows all of the elements recited in claim 1 and therefore, claim 1 is rejected.

Regarding claim 2, Tavallaei discloses the use of a peripheral component interconnect device(Figure 1, Component 34). Tavallaei shows all of the elements recited in claim 2 and therefore, claim 2 is rejected.

Regarding claim 3, Tavallaei discloses a PCI bus coupled in between the PCI device and the switch. Tavallaei further discloses the PCI bus supporting a plurality of additional PCI devices(Column 6, Lines 47-53). Tavallaei shows all of the elements recited in claim 3 and therefore, claim 3 is rejected.

Claims 9-12, 14-21, and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig et al.(US Patent 5,944,809), hereinafter referred to as Olarig.

Regarding claim 9, Olarig discloses a method for delivering an interrupt request in a computer system comprising of receiving an interrupt request, determining a local PIC to receive the interrupt request and transmitting request to that local PIC(Column 9, Lines 57-65). Olarig shows all of the elements recited in claim 9 and therefore, claim 9 is rejected.

Regarding claim 10, Olarig discloses a method of determining a processor to receive an interrupt request(Column 9, Lines 57-65), Olarig shows all of the elements recited in claim 10 and therefore, claim 10 is rejected.

Regarding claim 11, Olarig discloses a method of comparing a priority of the processor's task with that of the IRQ(Column 10, Lines 8-10). Olarig shows all of the elements recited in claim 11 and therefore, claim 11 is rejected.

Regarding claim 12, Olarig discloses a method for interrupting the processor(Column 10, Lines 10-13). Olarig shows all of the elements recited in claim 12 and therefore, claim 12 is rejected.

Regarding claim 14, Olarig discloses an interrupt request that is a broadcast interrupt(Column 9, Lines 56-67, and Column 10, Lines 1-7). Olarig shows all of the elements recited in claim 14 and therefore, claim 14 is rejected.

Regarding claim 15, Olarig discloses the use of an end of interrupt register to indicate the end of processing of an interrupt(Column 7, Lines 50-55). Olarig shows all of the elements recited in claim 15 and therefore, claim 15 is rejected.

Regarding claim 16, Olarig discloses that a PCI device generates an interrupt request since Olarig discloses interrupts being received from their sources through the PCI bus, which would indicate interrupt requests from PCI devices(Column 3, Lines 24-30). Olarig shows all of the elements recited in claim 16 and therefore, claim 16 is rejected.

Regarding claim 17, Olarig discloses that the interrupt request is generated by a processor, which is handled by LOPICS(Column 7, Lines 28-30). Olarig shows all of the elements recited in claim 17 and therefore, claim 17 is rejected.

Regarding claim 18, Olarig discloses a method for delivering an interrupt request in a computer system comprising of receiving an interrupt request, determining a local

APIC to receive the interrupt request and transmitting request to that local APIC(Column 9, Lines 57-65). Olarig shows all of the elements recited in claim 18 and therefore, claim 18 is rejected.

Regarding claim 19, Olarig discloses a method of determining a processor to receive an interrupt request(Column 9, Lines 57-65), Olarig shows all of the elements recited in claim 19 and therefore, claim 19 is rejected.

Regarding claim 20, Olarig discloses a method of comparing a priority of the processor's task with that of the IRQ(Column 10, Lines 8-10). Olarig shows all of the elements recited in claim 20 and therefore, claim 20 is rejected.

Regarding claim 21, Olarig discloses a method for interrupting the processor(Column 10, Lines 10-13). Olarig shows all of the elements recited in claim 21 and therefore, claim 21 is rejected.

Regarding claim 23, Olarig discloses an interrupt request that is a broadcast interrupt(Column 9, Lines 56-67, and Column 10, Lines 1-7). Olarig shows all of the elements recited in claim 23 and therefore, claim 23 is rejected.

Regarding claim 24, Olarig discloses the use of an end of interrupt register to indicate the end of processing of an interrupt(Column 7, Lines 50-55). Olarig shows all of the elements recited in claim 24 and therefore, claim 24 is rejected.

Regarding claim 25, Olarig discloses that a PCI device generates an interrupt request since Olarig discloses interrupts being received from their sources through the PCI bus, which would indicate interrupt requests from PCI devices(Column 3, Lines 24-

30). Olarig shows all of the elements recited in claim 25 and therefore, claim 25 is rejected.

Regarding claim 26, , Olarig discloses that the interrupt request is generated by a processor, which is handled by LOPICS(Column 7, Lines 28-30). Olarig shows all of the elements recited in claim 26 and therefore, claim 26 is rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei, in view of Neal et al.(US Patent 6,119,191), hereinafter referred to as Neal.

Regarding claim 4, Tavallaei discloses of an input/output hub(Figure 1, Component 28) coupled between the PCI bus and the port switch. Tavallaei does not

disclose multiple PCI hubs connected to the input/output hub. However, Neal discloses of multiple PCI hubs connected to hub(Figure 5). Therefore, it would have been obvious to combine the teachings of Tavallaei with the teachings of Neal because this would allow more PCI devices to be connected.

Regarding claim 5, Tavallaei discloses a second pair of node controllers coupled to a switch(Figure 1). Tavallaei shows all of the elements recited in claim 5.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei and Neal as applied to claims 4-5 above, and further in view of Olarig.

To analyze claim 7, examiner assumes claim 7 depends on claim 6.

Regarding claims 6 and 7, Tavallaei and Neal do not disclose the use of an additional switch connected to the first input/output hub. However, Olarig discloses the use of multiple switches(Column 8, Lines 5-13). Therefore it would be obvious to combine the teachings of Tavallaei and Neal with the teachings of Olarig to have a second port switch connected to the first input/output hub because it would provide twice as much throughput and maximum bandwidth.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei, Neal, and Olarig as applied to claims 4-7 above, and further in view of Deshpande et al.(US Patent 6,606,676), hereinafter referred to as Deshpande.

Regarding claim 8, Tavallaei does not disclose the use of a second input/output hub. However, in view of Neal, it would have been obvious to include a second input/output hub connected to a second port switch since this would allow the expandability of more PCI hubs connected.

Tavallaei does not disclose the use of 4 processors coupled to a node controller. However, Deshpande discloses the use of multiple processors per node(Column 3, Lines 37-42). Deshpande's node controller performs a similar function to that of Tavallaei's local PIC. Therefore, it would have been obvious to combine the teachings of Tavallaei, Neal, and Olarig with the teachings of Deshpande to support multiple processors per node because it would reduce traffic on the bus shared between the nodes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,701,495 given to Arndt et al. discloses a scalable system interrupt structure for a multi-processing system. The interrupt mechanism is separated into two layers, an interrupt routing layer and an interrupt presentation layer.

US Patent 6,148,361 given to Carpenter et al. discloses interrupt architecture. computer system that includes at least 2 nodes coupled by a node interconnect. The system can handle both external and interprocessor interrupts.

US Patent 6,205,508 given to Bailey et al. discloses a method for distributing interrupts in a multi-processor system.

US Patent 5,758,169 given to Nizar et al. discloses a protocol for interrupt bus arbitration in a multi-processor system. The protocol governs the interrupt bus and determines a lowest priority processor to handle an interrupt.

US Patent 6,470,408 given to Morrison et al. discloses an apparatus and method for delivering interrupts via an APIC bus. The apparatus includes a bridge couple to the processor and an APIC bus. The bridge monitors the system bus for interrupts, converts to APIC messages, and sends it to the APIC bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

NGP

MARK H. RINEHART
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